In the claims:

Please delete claim 11 and amend claims 7, 12 as follows:

1. (original) A variable capacitor comprising:

first terminal means for applying a variable capacitance to another circuit, the first terminal means having a source voltage;

substrate connection means for connecting to a substrate to bias the substrate;

composite gate means, having a plurality of gate segments formed over the substrate, for inducing formation of a conducting channel in the substrate under a gate segment when a gate-segment voltage of the gate segment exceeds the source voltage by a threshold voltage, but for not forming the conducting channel when the gate-segment voltage of the gate segment does not exceed the source voltage by the threshold voltage;

source means, formed in the substrate but having an opposite polarity to the substrate, for connecting conducting channels under the gate segments to the first terminal means and for biasing the conducting channels under the substrate to the source voltage of the first terminal means;

variable voltage means for generating a first voltage that can be varied to adjust a capacitance value of the variable capacitance; and

multi-voltage means, coupled between the variable voltage means and a second voltage, for generating a plurality of voltages between the first and second voltages;

wherein the plurality of voltages are each applied to a different one of the gate segments whereby the gate segments are biased to a plurality of differing gate-segment biases between the first and second voltages,

whereby the capacitance value at the first terminal means is increased by adjusting the first voltage, causing additional gate segments to form conducting channels that increase capacitance.

2. (original) The variable capacitor of claim 1 wherein the second voltage is ground;

wherein the variable capacitance includes channel-to-substrate capacitances of the conducting channels.

3. (original) The variable capacitor of claim 2 wherein the multi-voltage means comprises a plurality of resistors in series between the first and second voltages, with connections to a gate segment made between a pair of adjacent resistors in the plurality of resistors.

4. (original) The variable capacitor of claim 3 wherein a pair of adjacent gate segments are separated by a common source segment of the source means.

5. (original) The variable capacitor of claim 1 wherein the capacitance value is linearly proportional to the first voltage.

6. (original) The variable capacitor of claim 1 wherein the second voltage is ground, and the first voltage is a voltage that is above the threshold voltage.

7. (currently amended) A gated-diode variable capacitor comprising:
a gate formed over a thin insulator that separates the gate from a substrate;
a source formed in the substrate on a source side of the gate;
a substrate tap for connecting a substrate bias voltage to a substrate under the gate;
an upper-gate contact to the gate for applying an upper voltage to an upper portion of the gate; ~~and~~
a lower-gate contact to the gate for applying a lower voltage to a lower portion of the gate; and
a drain formed in the substrate on a drain side of the gate opposite the source side;
wherein the drain is connected to the source by a metal line and contacts;
wherein the upper voltage is higher than the lower voltage, wherein a gate-to-source voltage varies along the gate;
wherein a source bias voltage applied to the source, the upper voltage, and the lower voltage cause an inverted portion of the gate to have an inversion layer formed in the substrate under the inverted portion, and a non-inverted portion of the gate to

not ~~have a inversion~~ have an inversion layer formed in the substrate under the non-inverted portion;

wherein a capacitance per unit area of the inverted portion is higher than a capacitance per unit area of the non-inverted portion;

wherein capacitance of the variable capacitor measured from the source to the substrate is adjustable by adjusting a ratio of an area of the inverted portion to the area of the non-inverted portion.

whereby the source and the drain are both coupled to the source bias voltage and, ~~whereby~~ capacitance is adjustable by adjusting areas of inverted and non-inverted regions under the gate.

8. (original) The gated-diode variable capacitor of claim 7 wherein the substrate bias voltage is ground, the substrate is a p-type substrate, the upper voltage is more than a transistor threshold above the source bias voltage but the lower voltage is less than the transistor threshold above the source bias voltage or is below the source bias voltage.

9. (original) The gated-diode variable capacitor of claim 7 further comprising:

a variable voltage generator, coupled to the upper-gate contact, to vary the upper voltage applied to the gate;

wherein the lower voltage is ground or a fixed voltage between ground and a transistor threshold voltage.

10. (original) The gated-diode variable capacitor of claim 7 further comprising:

a fixed voltage generator, coupled to the upper-gate contact, to fix the upper voltage applied to the gate;

a variable voltage generator, coupled to the source by a source contact, to vary the source bias voltage applied to the source;

wherein the lower voltage is ground or a fixed voltage between ground and a transistor threshold voltage.

11. (canceled)

12. (currently amended) The gated-diode variable capacitor of ~~claim 11~~ claim 7 wherein the gate comprises a plurality gate arms biased to different voltages between the upper voltage and the lower voltage, the gate arms being electrically isolated from one another,

wherein gate current flow is blocked by electrical isolation of the gate arms.